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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,904	02/17/2004	Masahiro Ishida	02008.071003	9608

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EXAMINER
LOUIE, OSCAR A

ART UNIT	PAPER NUMBER
2436	

NOTIFICATION DATE	DELIVERY MODE
01/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/779,904	ISHIDA ET AL.	
	Examiner	Art Unit	
	OSCAR A. LOUIE	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,16 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,16 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This final action is in response to the amendment filed on 10/31/2008. Claims 4, 16, & 27 are pending and have been considered as follows.

Examiner Note

In light of the applicants' amendments, the examiner hereby withdraws his previous Claim Objections with respect to Claims 4, 16, & 27 and withdraws his previous 35 U.S.C. 101 rejections with respect to Claims 16 & 27.

Claim Objections

1. Claims 16 & 27 are objected to because of the following informalities:

- Claim 16 lines 3, 4, 6, 10, & 14 recite the term "for" which should be "…configured to…" as the current claim language appears to be intended use;
- Claim 27 3, 4, 6, 10, 13, & 16 lines recite the term "for" which should be "…configured to…" as the current claim language appears to be intended use;

> *The subject matter of a properly construed claim is defined by the terms that limit its scope. It is this subject matter that must be examined. As a general matter, the grammar and intended meaning of terms used in a claim will dictate whether the language limits the claim scope. Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim:*
> *(A) statements of intended use or field of use,*
> *(B) "adapted to" or "adapted for" clauses,*

(C) "wherein" clauses, or
(D) "whereby" clauses.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 16, & 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugasawara (US-6043672-A).

Claims 4 & 16:

Sugasawara discloses a fault analysis method & apparatus of/configured to presuming/presume a fault location of a semiconductor IC comprising,

- "applying a power supply voltage to said semiconductor IC" (i.e. "A selectable power supply line for providing power to a particular section of the integrated circuit is activated by an enable signal provided to a selectable power supply switch coupled to the selectable power supply line") [column 3 lines 28-32];

- "supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];
- "the electrical potentials at the one or more locations are expected to change once the test pattern sequence is supplied" (i.e. "Defects in integrated circuits take many forms, some of which are test pattern sensitive…Quiescent current tests differ in that current is sensed rather than voltage, providing a simple means to monitor the entire circuit or portions thereof for over-current conditions") [column 1 lines 64-65 & column 2 lines 25-28];
- "measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits") [column 2 lines 14-18];
- "determining whether said transient current shows abnormality or not" (i.e. "the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits. Such quiescent current tests are effective in detecting many faults that would otherwise not be found by other test strategies") [column 2 lines 16-20];

- "presuming a fault location out of said fault location list based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];
- "where the transient power supply current shows abnormality and said fault location list" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];
- "said transient power supply current is determined to be abnormal in a case that the time integral of said transient power supply current is over a predetermined value in said step of determining" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but Sugasawara does not explicitly disclose,

- "storing a fault location list for the test pattern sequence," although Sugasawara does suggest an automated test equipment that would store test pattern sequences and which portions of the semiconductor integrated circuit have been isolated for testing, as recited below;
- "wherein the fault location list includes one or more locations of components in said IC," although Sugasawara does suggest several components of a semiconductor integrated circuit that are tested for defects, as recited below;

however, Sugasawara does disclose,

- "automated test equipment (ATE)" [column 5 line 11];
- "CMOS circuits use complementary p-channel metal-oxide-semiconductor field-effect (PMOS) transistors and n-channel metal-oxide-semiconductor field-effect (NMOS) transistors… Gate oxide defects, drain to source current leaks (punch-through), and p-n junction current leaks (such as drain or source to diffusion current leaks)" [column 1 lines 36-39, 66-67 & column 2 line 1];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "storing a fault location list for the test pattern sequence" and "wherein the fault location list includes one or more locations of components in said IC," in the invention as disclosed by Sugasawara since predetermined reference values or test limits would typically be stored within the testing device in order to be compared to the resulting value(s).

Claim 27:

Sugasawara discloses a fault analysis apparatus configured to presume a fault location of semiconductor IC comprising,

- "a power supply for applying a power supply voltage to said semiconductor IC" (i.e. "A selectable power supply line for providing power to a particular section of the integrated circuit is activated by an enable signal provided to a selectable power supply switch coupled to the selectable power supply line") [column 3 lines 28-32];
- "a test pattern sequence input unit for supplying a test pattern sequence comprising a plurality of test patterns to said semiconductor IC" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are

performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];

- "the electric potentials at the one or more locations are expected to change once the test pattern sequence is supplied" (i.e. "Defects in integrated circuits take many forms, some of which are test pattern sensitive…Quiescent current tests differ in that current is sensed rather than voltage, providing a simple means to monitor the entire circuit or portions thereof for over-current conditions") [column 1 lines 64-65 & column 2 lines 25-28];
- "an integral transient power supply current measuring unit for measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits") [column 2 lines 14-18];
- "a fault detector for determining that said transient power supply current is abnormal in a case that the time integral of said transient power supply current is over a predetermined value" (i.e. "the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits. Such quiescent current tests are effective in detecting many faults that would otherwise not be found by other test strategies") [column 2 lines 16-20];

- "a fault location presuming unit for presuming a fault location out of said fault location list based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];
- "where the transient power supply current shows abnormality and said fault location list" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but Sugasawara does not explicitly disclose,

- "a fault location list memory unit for storing a fault location list for the test pattern sequence," although Sugasawara does suggest an automated test equipment that would store test pattern sequences and which portions of the semiconductor integrated circuit have been isolated for testing, as recited below;
- "wherein the fault location list includes one or more locations of components in said IC," although Sugasawara does suggest several components of a semiconductor integrated circuit that are tested for defects, as recited below;

however, Sugasawara does disclose,

- "automated test equipment (ATE)" [column 5 line 11];

- "CMOS circuits use complementary p-channel metal-oxide-semiconductor field-effect (PMOS) transistors and n-channel metal-oxide-semiconductor field-effect (NMOS) transistors… Gate oxide defects, drain to source current leaks (punch-through), and p-n junction current leaks (such as drain or source to diffusion current leaks)" [column 1 lines 36-39, 66-67 & column 2 line 1];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a means for storing a fault location list for the test pattern sequence" and "wherein the fault location list includes one or more locations of components in said IC," in the invention as disclosed by Sugasawara since predetermined reference values or test limits would typically be stored within the testing device in order to be compared to the resulting value(s).

Response to Arguments

4. Applicant's arguments filed 10/31/2008 have been fully considered but they are not persuasive.

- The applicants' arguments with respect to, "quiescent current and transient current are two very different concepts" and "quiescent current, as the term is used in Sugasawara, does not refer to the transient current of the claimed invention, which flows when the test pattern changes. In addition, unlike the claimed invention, Sugasawara requires electrical isolation of sections in the device under test in order to determine which sections are defective," have been carefully considered but are non-persuasive at this point in time;

- The examiner notes that although Sugasawara may not explicitly recite "transient current" and recites "quiescent current," it is reasonable to expect one of ordinary skill in the art at the time of the applicants' invention to utilize different defect detection methodologies that are common (i.e. "transient" and "quiescent") particularly if the steps and functionality are similar [see supporting cited NPL documents (as listed below) for additional evidence showing these two methodologies as having been well known in the art prior to the applicants' invention].

- The applicants' arguments with respect to, "Sugasawara fails to show or suggest at least 'measuring…a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not'" and "Sugasawara also fails to teach or suggest the "transient power supply current is determined to be abnormal in a case that the time integral of said transient power supply current is over a predetermined value" and "Sugasawara is completely silent with regard to using a time integral of said transient power supply current," have been carefully considered but are non-persuasive at this point in time;

  - The examiner notes that with respect to the "transient/quiescent current" aspects refer to the above argument response; and with respect to the "time integral" aspect(s), it is noted that it is reasonable to expect that analysis of a specific section of an integrated circuit suggests that a segment of time of observation is necessary to determine if there is/are defect(s);

- The examiner notes that it appears U.S. Patent No.'s US-6828815-B2 and US-6801049-B2 may create double patenting issues (that may be resolvable with a Terminal Disclaimer) with respect to this pending application, however, the examiner has not issued a double patenting rejection at this point in time since the applicants' claims appear to be directed to additional aspects not claimed but found within their Specification (i.e. pages 7-10 refers to additional details relating to "deleting" and "presuming" which are not claimed but appear to be integral aspects of the applicants' invention; pages 17-18 explicitly clarify that the IC is not just any IC but a "CMOS IC" which is not claim; pages 18-22, 24-28, etc. recite a multitude of formulas which if brought into the claim language may better distinguish the applicants' invention not just from the prior art of record, but from other co-pending or already Patented applications; pages 34-43, etc. recite additional non-claimed aspects with respect to what "time integrals" actually entail);

Conclusion

The prior art made of record and only relied upon as supporting evidence as of this correspondence is considered pertinent to the applicant's disclosure.

a. Hawkins et al. ("Quiescent power supply current measurement for CMOS IC defect detection") – quiescent/transient power supply current defect detection;

b. Sachdev et al. ("Defect detection with transient current testing and its potential for deep submicron CMOS ICs") – quiescent/transient power supply current defect detection;

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2400 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
01/09/2009

/Nasser G Moazzami/

Supervisory Patent Examiner, Art Unit 2436